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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,964	08/28/2003	Razak Hossain	03-LJ-011	1963

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,964	HOSSAIN, RAZAK	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *4-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/5/03, 2/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/604,964, and Response filed on 10/02/06. Applicants have provisionally elected claims 1-3 (Group 1) with traverse. Claims 4-19 (Groups 2-6) are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/02/2006.

2. The possible inventions of Groups 1 and 2 related to a circuit structure for testing using scan chains, but Group 2 includes additional utility, such as "a circuit for receiving a test vector for clocking into said scan chain elements". Because these inventions are distinct for the reasons given above and the search required for Group 1 is not required for Group 2, restriction for examination purposes as indicated is proper.

The possible inventions of Groups 1, 2 and 3 related to a circuit/method for reducing a leakage current, but Groups 1 and 2 include additional utilities, such as: "vector memory; a multiplexer and a circuit for receiving a test vector". Because these inventions are distinct for the reasons given above and the search required for Groups 1-2 is not required for Group 3, restriction for examination purposes as indicated is proper.

The possible inventions of Groups 1, 2, 3 and 4 related to a circuit/method for reducing a leakage current, but Group 4 includes additional utilities, such as "a test data vector; selectively clocking either a test data vector or a configuration vector into scan chain elements". Because these inventions are distinct for the reasons given above and

the search required for Group 4 is not required for Groups 1-3, restriction for examination purposes as indicated is proper.

The possible inventions of Groups 1, 2, 3, 4 and 5 related to a circuit/method for reducing a leakage current, but Group 5 includes additional utilities, such as "determining a vector having first states, which if applied to circuit elements of circuit results, in lower leakage currents than second states". Because these inventions are distinct for the reasons given above and the search required for Group 5 is not required for Groups 1-4, restriction for examination purposes as indicated is proper.

The possible inventions of Groups 1, 2, 3, 4, 5 and 6 related to a circuit/method for reducing a leakage current, but Group 6 includes additional utilities, such as "detecting whether said circuit is operating in either a first or a second operating mode; clocking test data into scan chin elements of said circuit when a second operating mode is detected". Because these inventions are distinct for the reasons given above and the search required for Group 6 is not required for Groups 1-5, restriction for examination purposes as indicated is proper.

As such, the restriction is hereby made final.

3. Examiner called Attorney Daniel E. Venglarik (Reg. No. 39,409) on 10/13/2006 regarding missing PTO form SB/08, no response from Attorney. Examiner did not consider IDS dated 02/18/2005 because Applicant did not provide standard PTO/SB/08 form. Applicant must present above form in the next Response for the future consideration.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-3 are rejected under 35 U.S.C. 102(a) as being unpatentable by Abdollahi et al. ("Leakage current reduction in sequential circuits by modifying the scan chains", fourth international symposium on 24-28 March 2003").

5. As to claims 1-3 Abdollahi discloses:

(1) A circuit, comprising:

circuit elements (pp. 1, 2, 5);

scan chain elements to contain a vector for selective application to said circuit elements (**In the scan-chain design**, the flip-flops are connected in such a way that **they enable two nodes of operation: normal node and test mode** – p.2 .. the following steps are used **to apply a test vector**: 1. The circuit is set **into test node by setting *test*=0**. 2, Shift the test vector into flip-flops ... 3. The circuit is configured to its **normal node by setting test=1**... - p. 3 ... a design technique for **applying the minimum leakage input to a sequential circuit** – Abstract, p. 1; the **sequential circuit comprises of a combinational circuit and a set of flip-flops** – p.2, Fig.2) (pp. 1, 2, 3);

a vector memory for containing a configuration vector (... **memory** ... is used for **storing the MLV/minimum leakage vector** – p. 4) which, when applied to said

circuit elements (a design technique for **applying the minimum leakage input to a sequential circuit** – Abstract, p. 1), configures said circuit elements into **a state** in which a leakage current is reduced (Having found the **minimum leakage pattern**/vector, one can use **this vector** to **drive the circuit** while in the **sleep mode** ... The **leakage current of a logic gate is a strong function of its input values** ... the input values **affect the number of OFF transistors in NMOS and PMOS** networks of a logic gate. For example, the **minimum leakage current of a two-input NAND gate** corresponds to the case, when **both its inputs are zero**. In this case, **both NMOS transistors** in the MMOS network **are off**, while **both PMOS transistors are on** – p. 2) (pp. 2, 3, 4); and

a multiplexer to select said configuration vector for loading into said scan chain elements (Having found the **minimum leakage pattern**/vector, one can use **this vector** to **drive the circuit** while in the **sleep mode. This requires the addition of some multiplexers at the primary inputs of the circuit. The multiplexers are controlled using a sleep signal**. – p. 2 ... the scan-based test methodology requires the modification of the circuit and addition of a test mode in which the **flip-flops are configured as one or more scan chains**. ... One way to add the new functionality into the flip-flops is through the addition of **a multiplexer with inputs *D* and Ds**, as shown in Fig. 3 ... The control input of the multiplexer is controlled by the test signal. This design is referred to as a **multiplexed-input scan** flip-flop – p. 3) (pp. 2-5);

a clock generator to clock said configuration vector into said scan chain elements (A simple way is **to shift in the *MLV***, from a memory (*m+k* bit shift register) into the first

m+k flip-flops via the *ScanIn* pin by **setting the circuit into the test mode and applying *m+k* clocks**. For this reason the sleep signal, generated by the power management unit, is combined with the test signal to construct the new control input of the multiplexed flip-flops. After shifting in the MLV, the clock signal can be disabled to avoid power dissipation in the flip-flops as depicted in Figure 5 – p. 3) (pp. 3-5);

(2) The circuit of claim 1 further comprising a sleep mode detector (pp. 3-5);

(3) The circuit of claim 2 further comprising a scan chain turn off circuit to turn off a clock to said scan chain elements after said configuration vector has been applied to said circuit elements (pp. 3-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

Nhuando
THUAN DO
Primary examiner.
10/25/06